WHAT IS CLAIMED IS:

1. An amplifier, comprising:

a first transistor driven by input voltage;

a second transistor driven by a first voltage, the second transistor being coupled to a first terminal of the first transistor; and

a third transistor stacked on the second transistor and driven by a second voltage, the third transistor being coupled to a second terminal of the first transistor, wherein the first transistor operates in an active region, and the second transistor operates in a linear region according to the second voltage and the third transistor.

2. The amplifier as claimed in claim 1, wherein the first voltage is applied when the input voltage passes through an offset DC voltage source that performs AC coupling and determines DC voltage.

3. The amplifier as claimed in claim 1, wherein the second voltage is applied when a third voltage having polarity opposite to that of the input voltage passes through an offset DC voltage source that performs AC coupling and determines DC voltage.

4. The amplifier as claimed in claim 1, wherein the second voltage is applied when a voltage applied to a contact node of the first transistor and the third transistor passes through an offset DC voltage source that performs AC coupling and determines DC voltage.

5. The amplifier as claimed in one of claims 2, wherein both ends of the offset DC voltage source are short-circuited.

6. The amplifier as claimed in one of claims 2, wherein the offset DC voltage source includes a capacitor coupled between both ends thereof and a resistor coupled between a DC voltage source and one end thereof.

7. An amplifier that outputs amplified output current according to input voltage, *comprising*:

a first transistor operating in an active region, a first current flowing through the first transistor according to the input voltage;

a second transistor driven by a first voltage, a second current flowing through the second transistor; and

a third transistor driven by a second voltage to secure a linear region operation of the second transistor, the third transistor being stacked on the second transistor to be coupled to the output terminal of the first transistor,

wherein the output current includes the first and second currents.

8. The amplifier as claimed in claim 7, wherein the first voltage corresponds to the sum of an offset DC voltage and an AC component bypassed input voltage.

9. The amplifier as claimed in claim 7, wherein the second voltage corresponds to the sum of an offset DC voltage and an AC component bypassed third voltage having polarity opposite to that of the input voltage.

10. The amplifier as claimed in claim 7, wherein the second voltage corresponds to the sum of an offset DC voltage and AC component bypassed voltage of the output terminal of the first transistor.

11. The amplifier as claimed in claim 7, wherein the second voltage corresponds to voltage at the output terminal of the first transistor.

12. A method for canceling nonlinearity in an amplifier having a first transistor operating in an active region according to input voltage and a second transistor driven by a first voltage, the method comprising:

applying a second voltage to a third transistor stacked on the second transistor to allow the second transistor to operate in a linear region; and

adding a first current flowing through the first transistor and a second current flowing through the second transistor.

13. The method as claimed in claim 12, wherein the first voltage corresponds to the sum of an offset DC voltage and AC component bypassed input voltage.